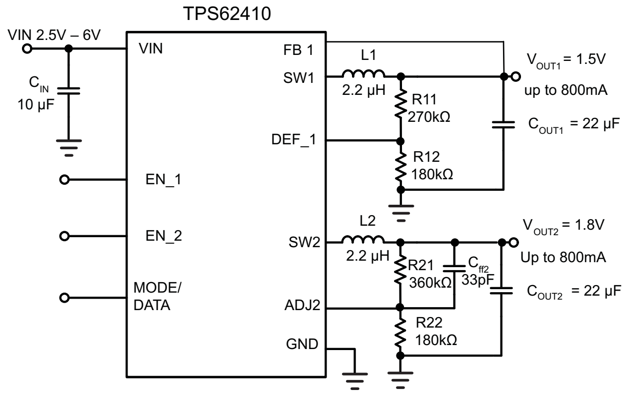
2.25MHz 2x800mA Dual Step Down Converter In Small 3x3mm QFN Package

FEATURES

- **High Efficiency—up to 95%**
- **V_{IN} Range From 2.5 V to 6 V**
- **2.25 MHz Fixed Frequency Operation**
- **Output Current 2 x 800mA**
- **Adjustable Output Voltage From 0.6 V to V_{IN}**
- **EasyScale™ Optional One Pin Serial Interface for Dynamic Output Voltage Adjustment**
- **Power Save Mode at Light Load Currents**
- **180° Out of Phase Operation**
- **Output Voltage Accuracy in PWM Mode ±1%**
- **Typical 32 μA Quiescent Current for both Converters**
- **100% Duty Cycle for Lowest Dropout**
- **Available in a 10-Pin QFN (3×3mm)**

APPLICATIONS

- **Cell Phones, Smart-phones**
- **PDAs, Pocket PCs**
- **OMAP™ and Low Power DSP Supply**
- **Portable Media Players**
- **Digital Radio**
- **Digital Cameras**



DESCRIPTION

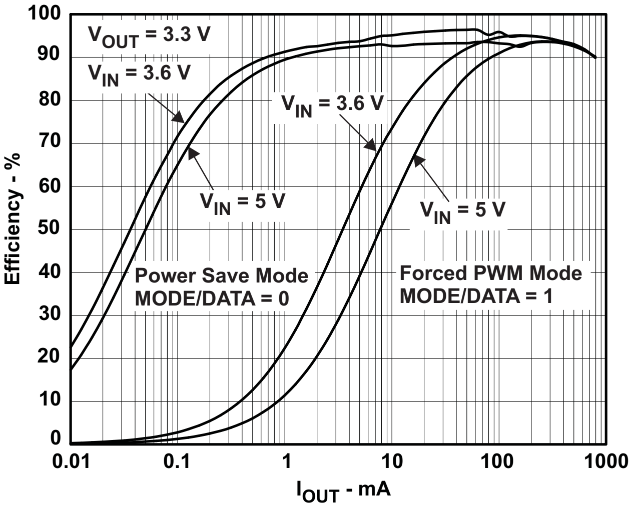
The TPS62410 device is a synchronous dual step-down DC-DC converter optimized for battery powered portable applications. It provides two independent output voltage rails powered by 1-cell Li-Ion or 3-cell NiMH/NiCD batteries. The device is also suitable to operate from a standard 3.3V or 5V voltage rail.

With an input voltage range of 2.5V to 6V, the TPS62410 is ideal to power portable applications like smart phones, PDAs, and other portable equipment.

With the EasyScale™ serial interface the output voltages can be modified during operation. It therefore supports Dynamic Voltage Scaling for low power DSP and processors.

The TPS62410 operates at 2.25MHz fixed switching frequency and enter the Power Save Mode operation at light load currents to maintain high efficiency over the entire load current range. For low noise applications the devices can be forced into fixed frequency PWM mode by pulling the MODE/DATA pin high. In the shutdown mode, the current consumption is reduced to 1.2μA. The device allows the use of small inductors and capacitors to achieve a small solution size.

The TPS62410 is available in a 10-pin leadless package (3×3mm QFN)



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ORDERING INFORMATION(1)

T_A	PART NUMBER (1)	DEFAULT OUTPUT VOLTAGE (2)		OUTPUT CURRENT	QFN (1) PACKAGE	ORDERING	PACKAGE MARKING
–40°C to 85°C	TPS62410	OUT1	Adjustable	800mA	DRC	TPS62410DRC	CAT
		OUT2		800mA			

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE	UNIT
	Input voltage range on V_{IN}(2)		–0.3 to 7	V
	Voltage range on EN, MODE/DATA, DEF_1		–0.3 to V_{IN} +0.3, ≤7	V
	Maximum Current into MODE/DATA		500	µA
	Voltage on SW1, SW2		–0.3 to 7	V
	Voltage on ADJ2, FB1		–0.3 to V_{IN} +0.3, ≤7	V
	ESD rating(3)	HBM Human body nodel	2	kV
		Charge device model	1	kV
		Machine model	200	V
$T_{J(max)}$	Maximum junction temperature		150	°C
T_A	Operating ambient temperature range		–40 to 85	°C
T_{stg}	Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

(3) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

DISSIPATION RATINGS

PACKAGE	$R_{\theta JA}$	POWER RATING FOR $T_A \le$ 25°C	DERATING FACTOR ABOVE T_A = 25°C
DRC	49°C/W	2050mW	21mW/°C

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Supply voltage	2.5		6	V
	Output voltage range for adjustable voltage	0.6		VIN	V
T_A	Operating ambient temperature	-40		85	°C
T_J	Operating junction temperature	-40		125	°C

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, V_{OUT} = 1.8V, EN = V_{IN}, MODE = GND, L = 2.2µH, C_{OUT} = 20µF, T_A = –40°C to 85°C typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage range		2.5		6.0	V
I_Q	Operating quiescent current	One converter, I_{OUT} = 0mA. PFM mode enabled (Mode = 0) device not switching, EN1 = 1 OR EN2 = 1		19	29	µA
		Two converter, I_{OUT} = 0mA. PFM mode enabled (Mode = 0) device not switching, EN1 = 1 AND EN2 = 1		32	48	µA
		I_{OUT} = 0mA, MODE/DATA = GND, for one converter, V_{OUT} 1.575V (1)		23		µA
		I_{OUT} = 0mA, MODE/DATA = V_{IN}, for one converter, V_{OUT} 1.575V (1)		3.6		mA
I_{SD}	Shutdown current	EN1, EN2 = GND, V_{IN} = 3.6V (2)		1.2	3	µA
		EN1, EN2 = GND, V_{IN} ramped from 0V to 3.6V (3)		0.1	1	
V_{UVLO}	Undervoltage lockout threshold	Falling		1.5	2.35	V
		Rising			2.4	
ENABLE EN1, EN2						
V_{IH}	High-level input voltage, EN1, EN2		1.2		V_{IN}	V
V_{IL}	Low-level input voltage, EN1, EN2		0		0.4	V
I_{IN}	Input bias current, EN1, EN2	EN1, EN2 = GND or VIN		0.05	1.0	µA
DEF_1 INPUT						
I_{IN}	Input biasd current DEF_1	DEF_1 = GND or VIN		0.01	1.0	µA
MODE/DATA						
V_{IH}	High-level input voltage, MODE/DATA		1.2		V_{IN}	V
V_{IL}	Low-level input voltage, MODE/DATA		0		0.4	V
I_{IN}	Input bias current, MODE/DATA	MODE/DATA = GND or VIN		0.01	1.0	µA
V_{OH}	Acknowledge output voltage high	Open drain, via external pullup resistor			V_{IN}	V
V_{OL}	Acknowledge output voltage low	Open drain, sink current 500µA	0		0.4	V
INTERFACE TIMING						
t_{Start}	Start time		2			µs
t_{H_LB}	High time low bit, logic 0 detection	Signal level on MODE/DATA pin is > 1.2V	2		200	µs
t_{L_LB}	Low time low bit, logic 0 detection	Signal level on MODE/DATA pin < 0.4V	2x t_{H_LB}		400	µs
t_{L_HB}	Low time high bit, logic 1 detection	Signal level on MODE/DATA pin < 0.4V	2		200	µs
t_{H_LB}	High time high bit, logic 1 detection	Signal level on MODE/DATA pin is > 1.2V	2x t_{L_HS}		400	µs
T_{EOS}	End of Stream	T_{EOS}	2			µs
t_{ACKN}	Duration of acknowledge condition (MODE/DATE line pulled low by the device)	V_{IN} 2.5V to 6V	400		520	µs
t_{valACK}	Acknowledge valid time				2	µs
$t_{timeout}$	Timeout for entering power save mode	MODE/DATA Pin changes from high to low			520	µs

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(1) Device is switching with no load on the output, L = 3.3µH, value includes losses of the coil

(2) These values are valid after the device has been already enabled one time (EN1 or EN2 = high) and supply voltage V_{IN} has not powered down.

(3) These values are valid when the device is disabled (EN1 and EN2 low) and supply voltage V_{IN} is powered up. The values remain valid until the device has been enabled first time (EN1 or EN2 = high). After first enable, Note 3 becomes valid.

ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 3.6V, V_{OUT} = 1.8V, EN = V_{IN}, MODE = GND, L = 2.2µH, C_{OUT} = 20µF, T_A = –40°C to 85°C typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCH							
$R_{DS(ON)}$	P-Channel MOSFET On-resistance, Converter 1,2		V_{IN} = V_{GS} = 3.6V		280	620	mΩ
I_{LK_PMOS}	P-Channel leakage current		V_{DS} = 6.0V			1	µA
$R_{DS(ON)}$	N-Channel MOSFET On-resistance Converter 1,2		V_{IN} = V_{GS} = 3.6V		200	450	mΩ
$I_{LK\_SW1/SW2}$	Leakage Current into SW1/SW2 Pin		Includes N-Chanel leakage currnet, V_{IN} = open, V_{SW} = 6.0V, EN = GND (4)		6	7.5	µA
I_{LIMF}	Forward Current Limit PMOS and NMOS	OUT 1/2 800mA	2.5V ≤ V_{IN} ≤ 6.0V	1.0	1.2	1.38	A
T_{SD}	Thermal shutdown		Increasing junction temperature		150		°C
	Thermal shudown hysteresis		Decreasing junction temperature		20		°C
OSCILLATOR							
fSW	Oscillator frequency		2.5V ≤ VIN ≤ 6.0V	2.0	2.25	2.5	MHz
OUTPUT							
V_{OUT}	Adjustable output votage range			0.6		V_{IN}	V
V_{ref}	Reference voltage				600		mV
$V_{OUT\ (PFM)}$	DC output voltage accuracy PFM mode, adjustable and fixed output voltage (5)		Voltage positioning active, MODE/DATA = GND, device operating in PFM mode, VIN = 2.5V to 5.0V (6) (7)	–1.5%	1.01x V_{OUT}	2.5%	
V_{OUT}			MODE/DATA = GND; device operating in PWM Mode VIN = 2.5V to 6.0V (7)	–1%	0%	1%	
			V_{IN} = 2.5V to 6.0V, Mode/Data = V_{IN} , Fixed PWM operation, 0mA < I_{OUT} < I_{OUTMAX} (8)	–1%	0%	1%	
	DC output voltage load regulation		PWM operation mode			0.5	%/A
$t_{Start\ up}$	Start-up time		Activation time to start switching (9)		170		µs
t_{Ramp}	V_{OUT} Ramp UP time		Time to ramp from 5% to 95% of V_{OUT}		750		µs

(4) At pins SW1 and SW2 an internal resistor of 1MΩ is connected to GND

(5) Output voltage specification does not include tolerance of external voltage programming resistors

(6) Configuration L typ 2.2µH, C_{OUT} typ 20µF, see parameter measurement information, the output voltage ripple depends on the effective capacitance of the output capacitor, larger output capacitors lead to tighter output voltage tolerance

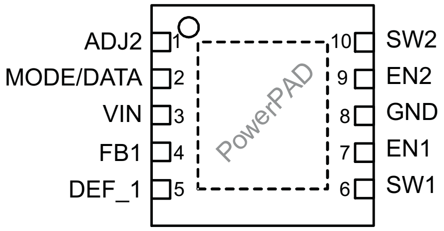
(7) In Power Save Mode, PWM operation is typically entered at I_{PSM} = V_{IN}/32Ω.

(8) For V_{OUT} > 2.2V, V_{IN} min = V_{OUT} +0.3V

(9) This time is valid if one converter turns from shutdown mode (EN2 = 0) to active mode (EN2 =1) AND the other converter is already enabled (e.g., EN1 = 1). In case both converters are turned from shutdown mode (EN1 and EN2 = low) to active mode (EN1 and/or EN2=1) a value of typ 80 µs for ramp up of internal circuits needs to be added. After t_{Start} the converter starts switching and ramps V_{OUT}.

DEVICE INFORMATION

PIN ASSIGNMENTS

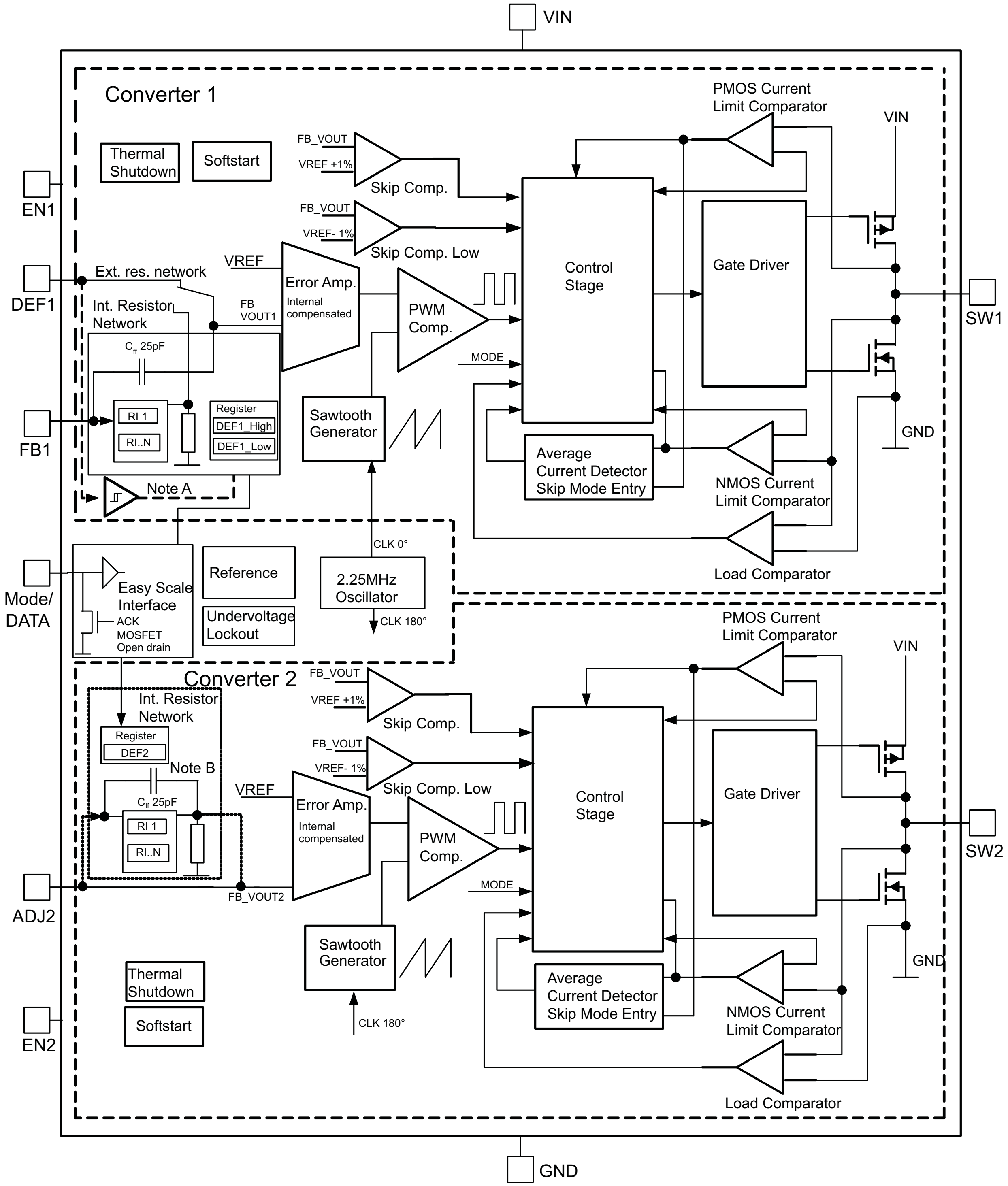


Top view DRC package

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO. (QFN)		
ADJ2	1	I	Input to adjust output voltage of converter 2. In adjustable version (TPS62410) connect a external resistor divider between VOUT2, this pin and GND to set output voltage between 0.6V and VIN. If EasyScale™ Interface is used for converter 2, this pin must be directly connected to the output.
MODE/DATA	2	I	This Pin has 2 functions: 1. Operation Mode selection: With low level, Power Save Mode is enabled where the device operates in PFM mode at light loads and enters automatically PWM mode at heavy loads. Pulling this PIN to high forces the device to operate in PWM mode over the whole load range. 2. EasyScale™ Interface function: One wire serial interface to change the output voltage of both converters. The pin has an open drain output to provide an acknowledge condition if requested. The current into the open drain output stage may not exceed 500µA. The interface is active if either EN1 or EN2 is high.
VIN	3	I	Supply voltage, connect to VBAT, 2.5V to 6V
FB1	4	I	Direct feedback voltage sense input of converter 1, connect directly to Vout 1. An internal feed forward capacitor is connected between this pin and the error amplifier. In case of fixed output voltage versions or when the Interface is used, this pin is connected to an internal resistor divider network.
DEF_1	5	I/O	This pin defines the output voltage of converter 1. The pin acts in TPS62410 as an analog input for output voltage setting via external resistors. In fixed default output voltage versions this pin is a digital input to select between two fixed default output voltages. In TPS62410 an external resistor network needs to be connected to this pin to adjust the default output voltage.
SW1	6		Switch Pin of Converter1. Connected to Inductor 1
EN1	7	I	Enable Input for Converter1, active high
GND	8	I	GND for both converters, this pin should be connected with the PowerPAD
EN2	9	I/O	Enable Input for Converter 2, active high
SW2	10		Switch Pin of Converter 2. Connected to Inductor 2
PowerPAD™			Connect to GND

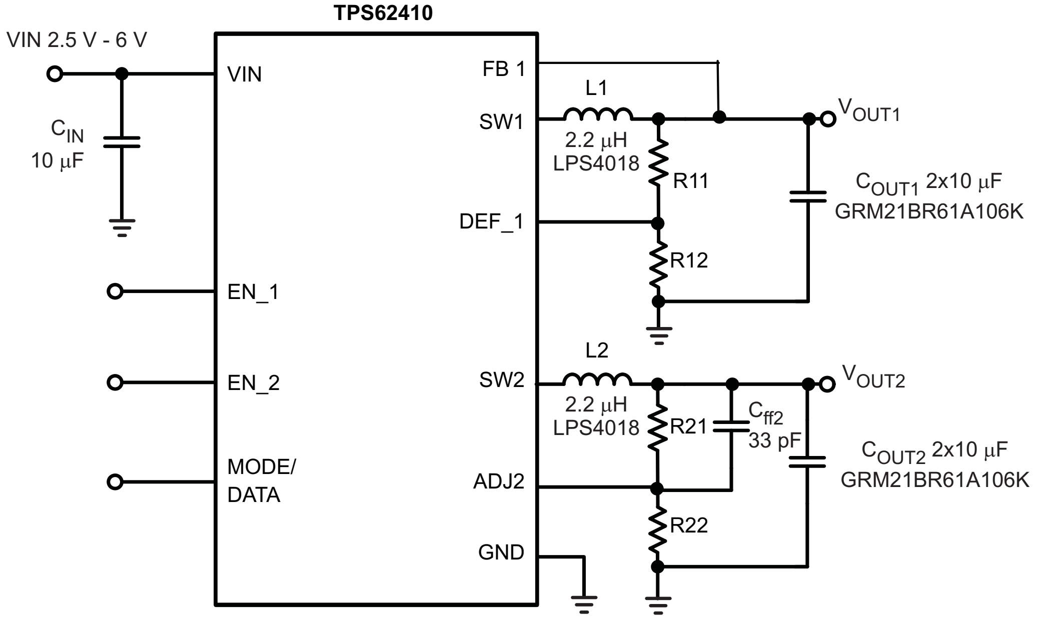
FUNCTIONAL BLOCK DIAGRAM



A. In fixed output voltage version, the PIN DEF_1 is connected to an internal digital input and disconnected from the error amplifier

B. To set the output voltage of Converter 2 via EasyScale Interface, ADJ2 pin must be directly connected to VOUT2

PARAMETER MEASUREMENT INFORMATION



TYPICAL CHARACTERISTICS

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Efficiency V_{OUT1} = 1.5V		2
Efficiency V_{OUT2} = 1.8V		3
Efficiency V_{OUT2} = 3.3V		4
Efficiency	vs V_{IN}	5, 6
DC Output Accuracy V_{OUT1} = 1.5V		7
DC Output Accuracy V_{OUT2} = 3.3V		8
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EFFICIENCY V_{OUT} = 1.2V

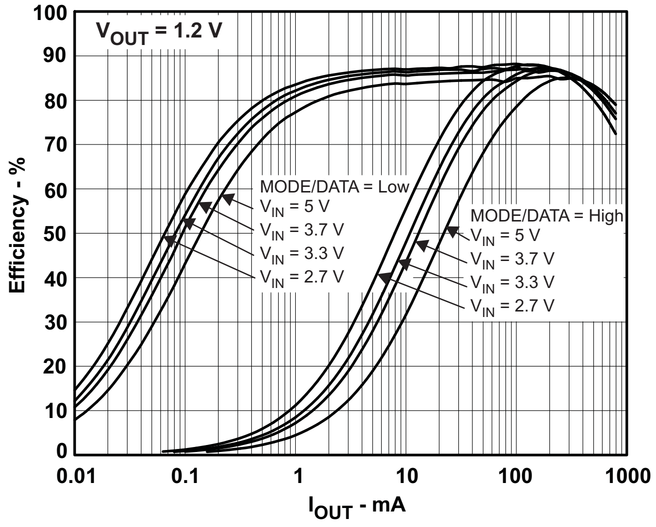


Figure 1.

EFFICIENCY V_{OUT} = 1.5V

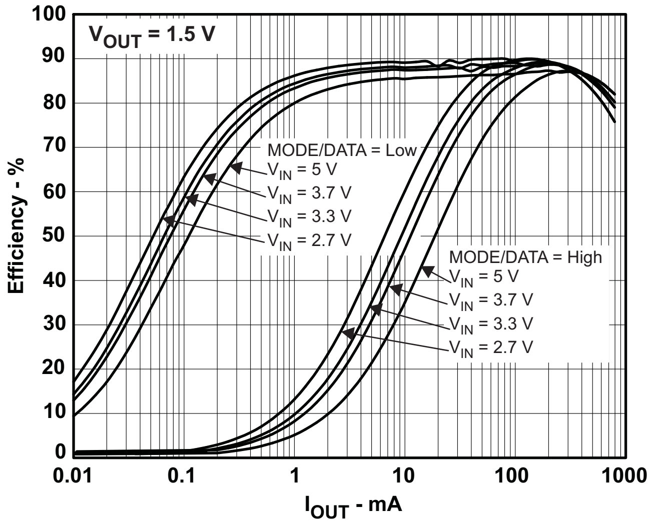


Figure 2.

EFFICIENCY V_{OUT2} = 1.8V

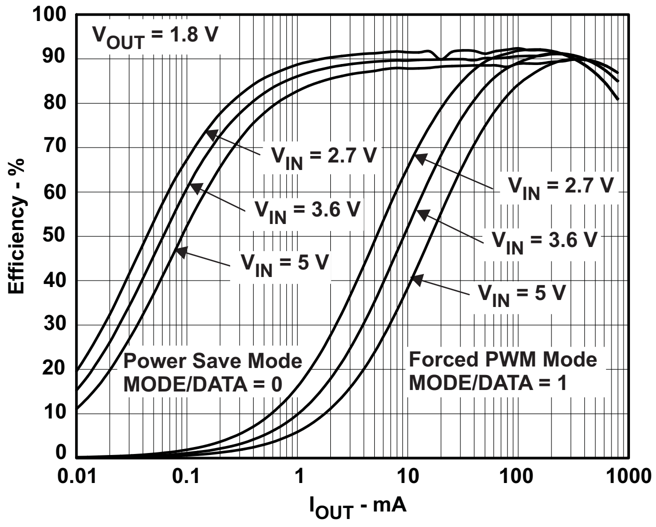


Figure 3.

EFFICIENCY V_{OUT2} = 3.3V

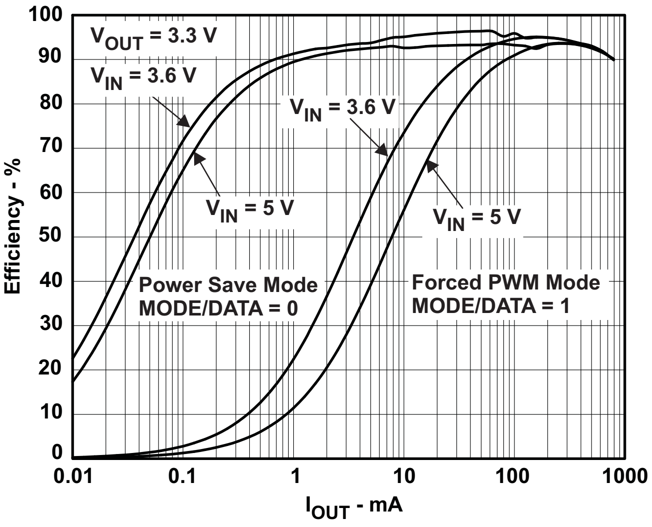


Figure 4.

EFFICIENCY vs V_{IN} , V_{OUT} = 1.575V

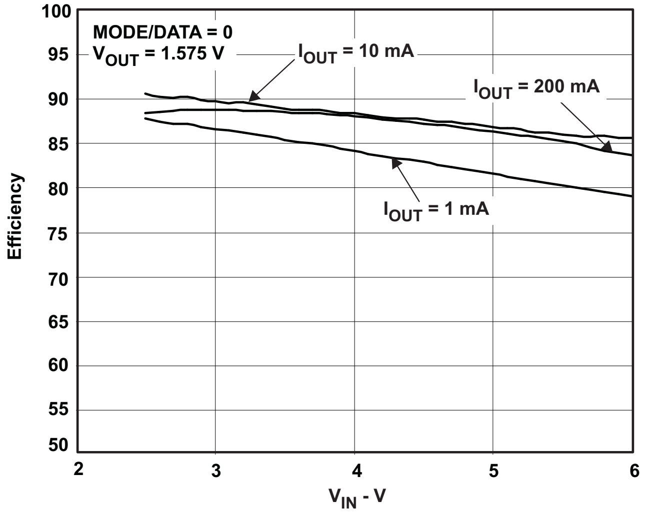


Figure 5.

EFFICIENCY vs V_{IN}, V_{OUT} = 3.3V

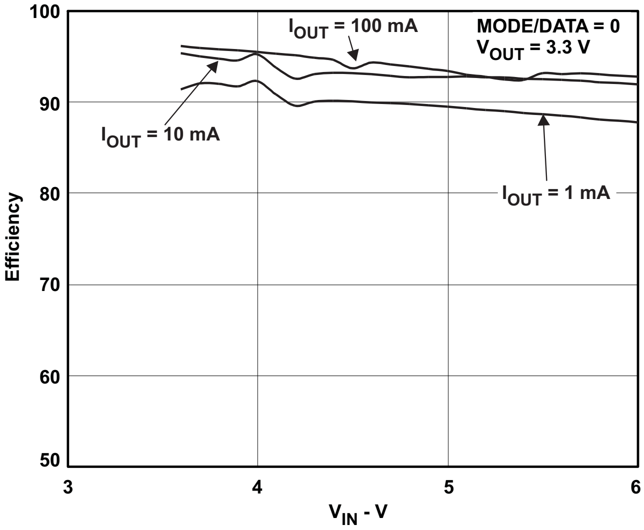


Figure 6.

DC OUTPUT ACCURACY V_{OUT1} = 1.5V

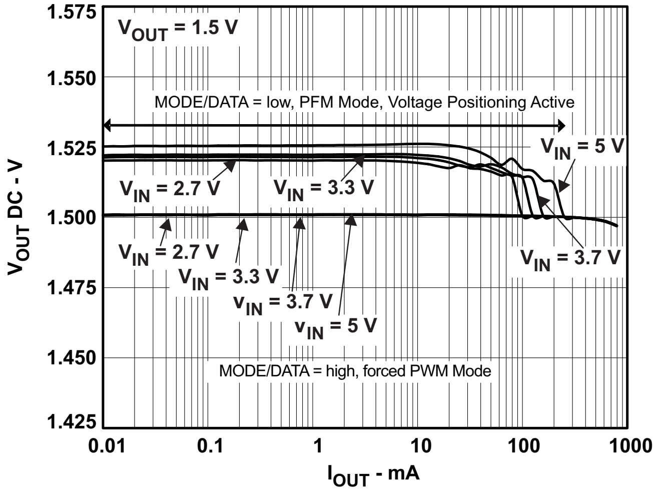


Figure 7.

DC OUTPUT ACCURACY V_{OUT2} = 3.3V

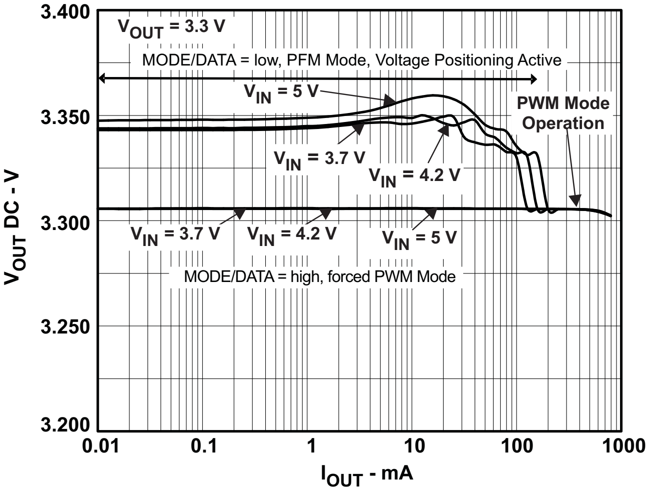


Figure 8.

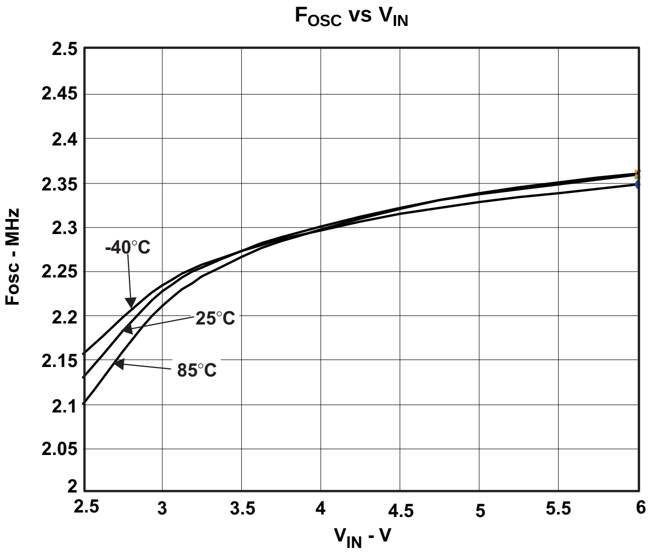


Figure 9.

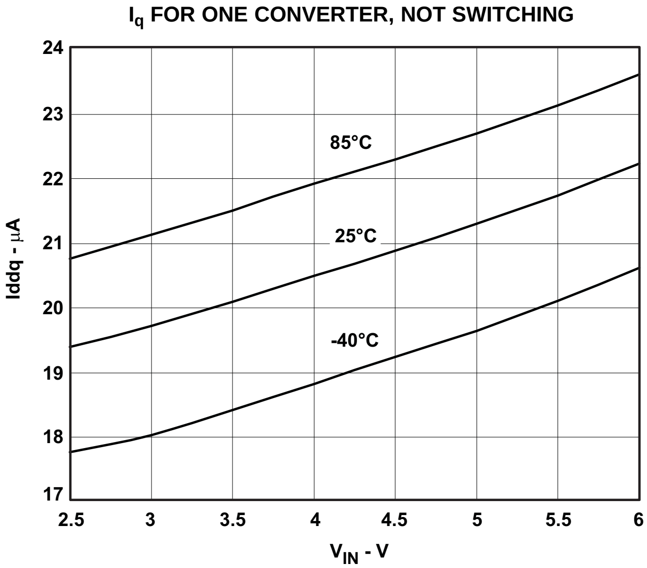


Figure 10.

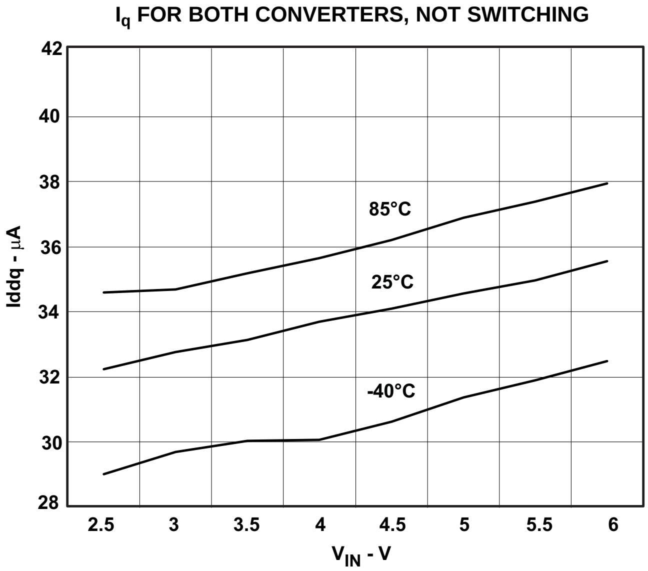


Figure 11.

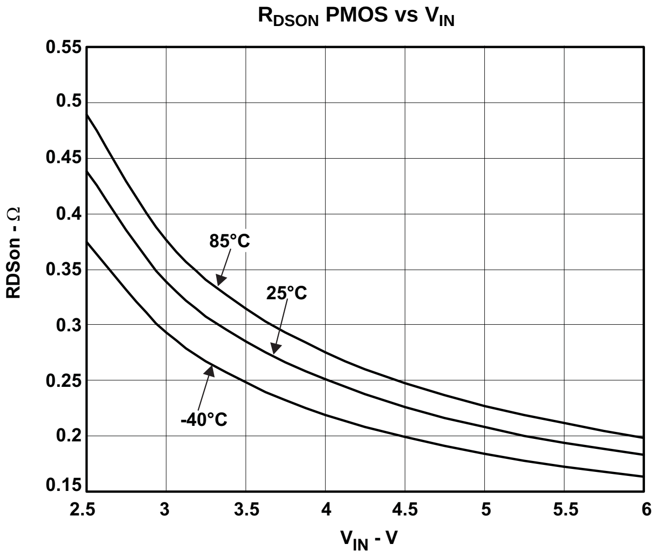


Figure 12.

R_{DSON} NMOS vs V_{IN}

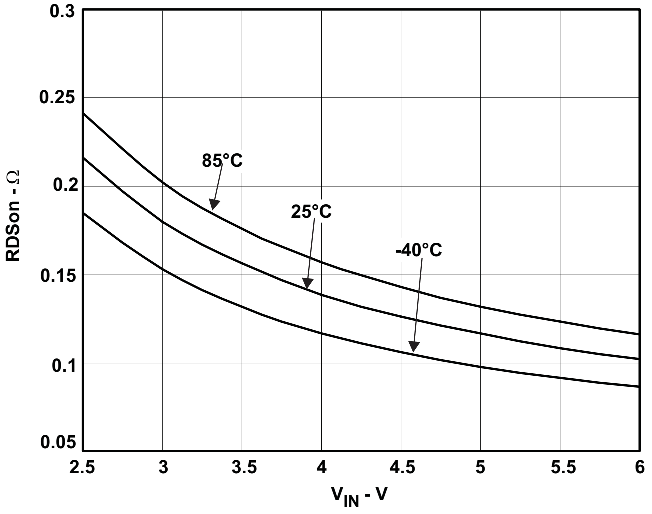
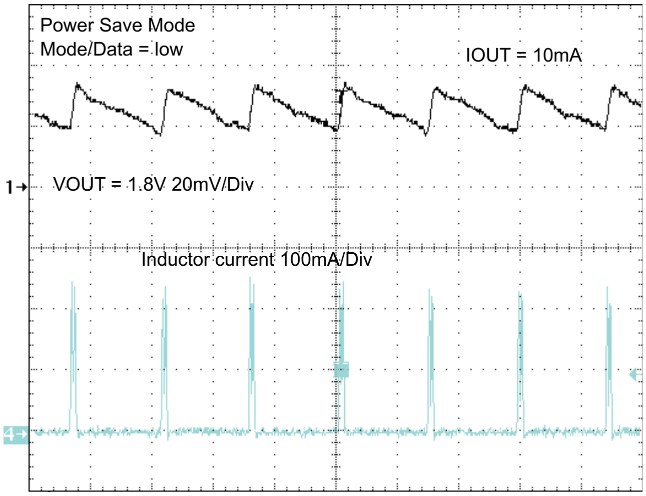


Figure 13.

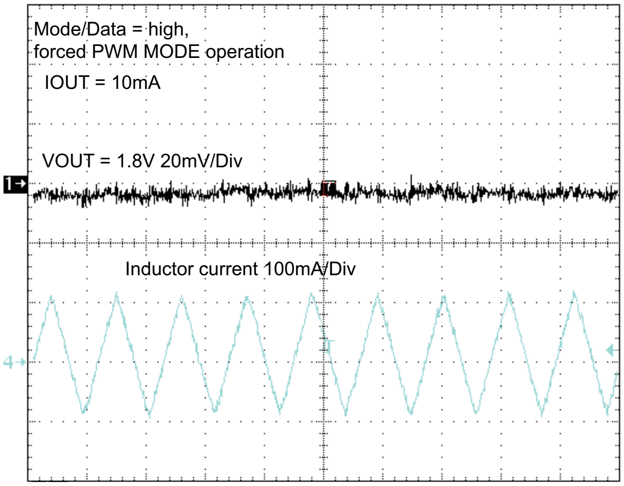
LIGHT LOAD OUTPUT VOLTAGE RIPPLE
IN POWER SAVE MODE



Time base - 10 µs/Div

Figure 14.

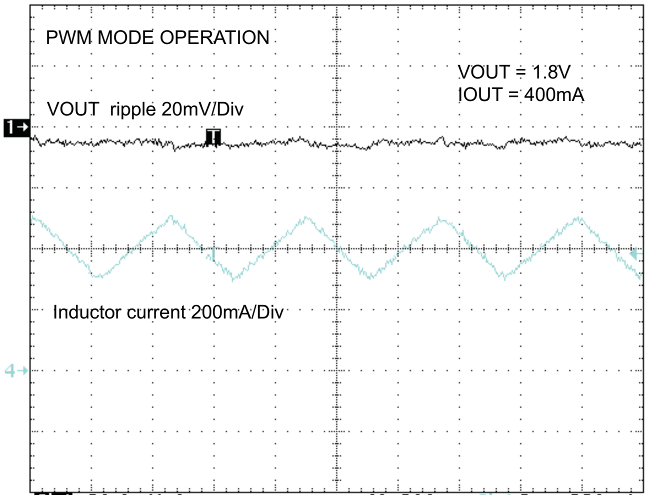
OUTPUT VOLTAGE RIPPLE
IN FORCED PWM MODE



Time base - 400 ns/Div

Figure 15.

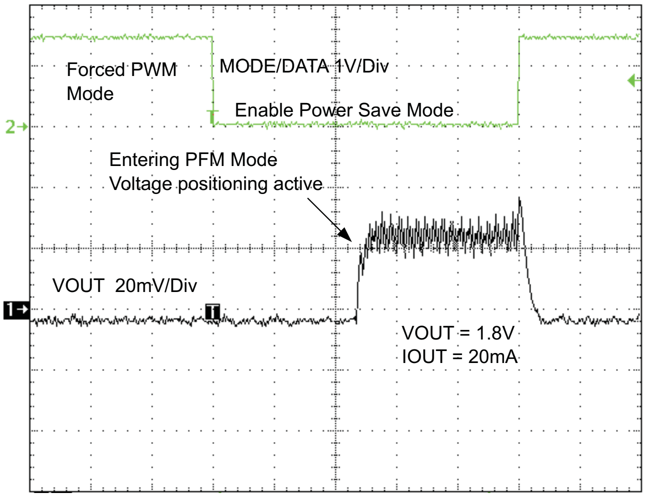
OUTPUT VOLTAGE RIPPLE
IN PWM MODE



Time base - 200 ns/Div

Figure 16.

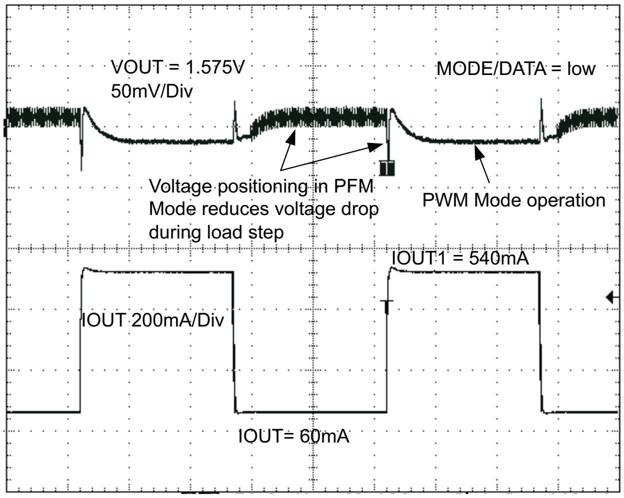
FORCED PWM/PFM MODE TRANSITION



Time base - 20 µs/Div

Figure 17.

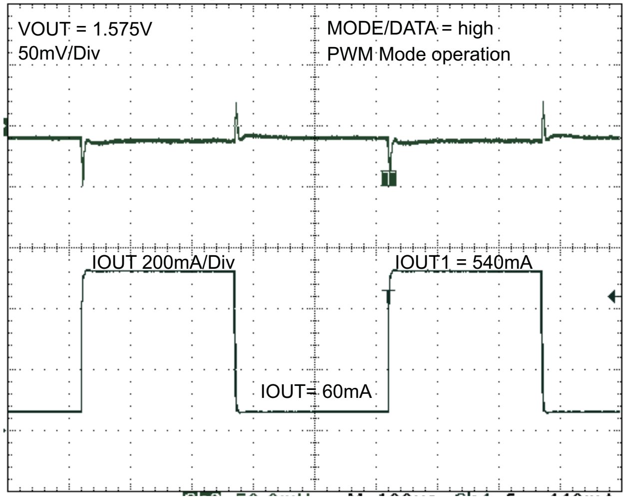
LOAD TRANSIENT RESPONSE PFM/PWM



Time base - 100 µs/Div

Figure 18.

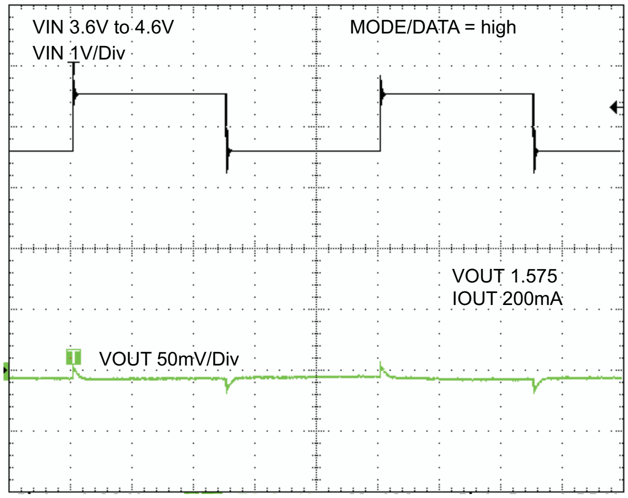
LOAD TRANSIENT RESPONSE PWM OPERATION



Time base - 100 µs/Div

Figure 19.

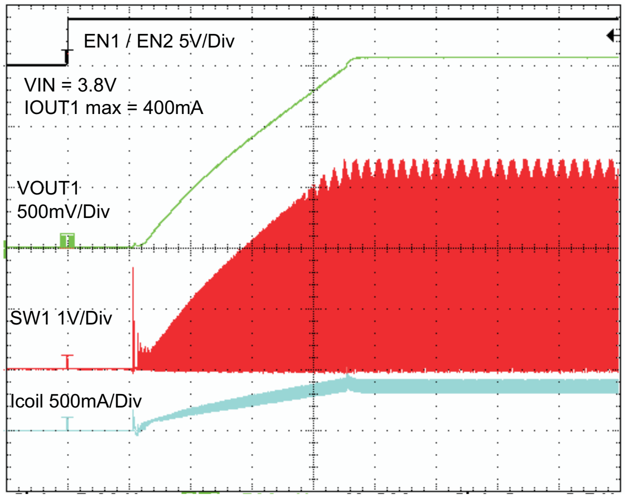
LINE TRANSIENT RESPONSE



Time base - 400 µs/Div

Figure 20.

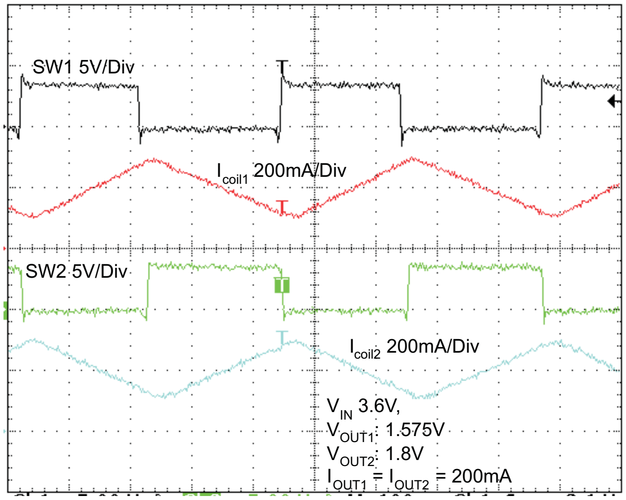
STARTUP TIMING ONE CONVERTER



Time base - 200 µs/Div

Figure 21.

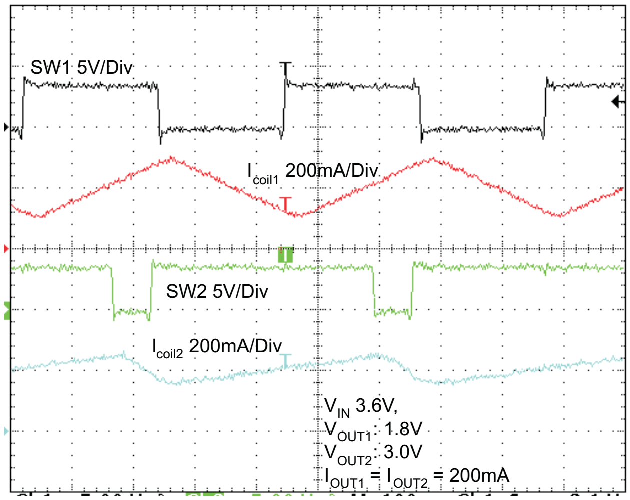
TYPICAL OPERATION V_{IN} = 3.6V, V_{OUT1} = 1.575V, V_{OUT2} = 1.8V



Time base - 100 ns/Div

Figure 22.

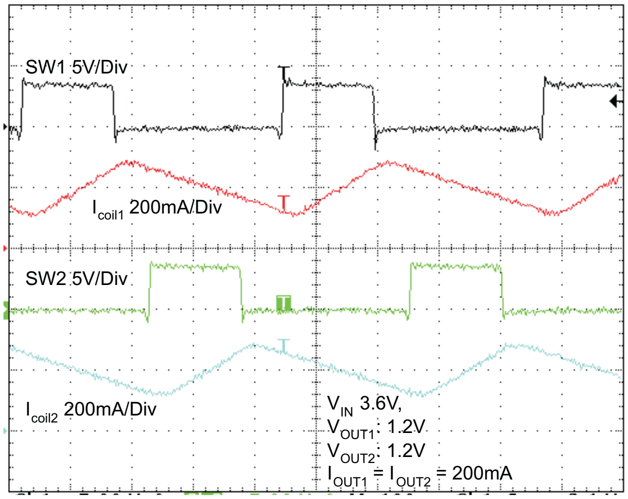
TYPICAL OPERATION V_{IN} = 3.6V, V_{OUT1} = 1.8V, V_{OUT2} = 3.0V



Time base - 100 ns/Div

Figure 23.

TYPICAL OPERATION V_{IN} = 3.6V, V_{OUT1} = 1.2V, V_{OUT2} = 1.2V



Time base - 100 ns/Div

Figure 24.

V_{OUT1} CHANGE WITH EASYSCALE

DETAILED DESCRIPTION

OPERATION

The TPS62410 includes two synchronous step-down converters. The converters operate with typically 2.25MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. If Power Save Mode is enabled, the converters automatically enter Power Save Mode at light load currents and operate in PFM (Pulse

DETAILED DESCRIPTION (continued)

Frequency Modulation). During PWM operation the converters use a unique fast response voltage mode controller scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the P-channel MOSFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch.

Each converter integrates two current limits, one in the P-channel MOSFET and another one in the N-channel MOSFET. When the current in the P-channel MOSFET reaches its current limit, the P-channel MOSFET is turned off and the N-channel MOSFET is turned on. If the current in the N-channel MOSFET is above the N-MOS current limit threshold, the N-channel MOSFET remains on until the current drops below its current limit. The two DC-DC converters operate synchronized to each other. A 180° phase shift between converter 1 and converter 2 decreases the input RMS current.

Converter 1

In the adjustable output voltage version TPS62410 the converter 1 output voltage can be set via an external resistor network on PIN DEF_1, which operates as an analog input. In this case, the output voltage can be set in the range of 0.6V to VIN V. The FB1 Pin must be directly connected to the converter 1 output voltage VOUT1. It feeds back the output voltage directly to the regulation loop.

The output voltage of converter 1 can also be changed by the EasyScale serial Interface. This makes the device very flexible for output voltage adjustment. In this case, the device uses an internal resistor network.

Converter 2

In the adjustable output voltage version TPS62410, the converter 2 output voltage is set by an external resistor divider connected to ADJ2 Pin and uses an external feed forward capacitor of 33pF.

It is also possible to change the output voltage of converter 2 via the EasyScale Interface. In this case, the ADJ2 Pin must be directly connected to converter 2 output voltage VOUT2. At TPS62410 no external resistor network may be connected.

POWER SAVE MODE

The Power Save Mode is enabled with Mode/Data Pin set to 0 for both converters. If the load current of a converter decreases, this converter will enter Power Save Mode operation automatically. The transition to Power Save Mode of a converter is independent from the operating condition of the other converter. During Power Save Mode the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current to maintain high efficiency. The converter will position the output voltage in PFM mode to typically 1.01xVOUT. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

In order to optimize the converter efficiency at light load the average inductor current is monitored. The device changes from PWM Mode to Power Save Mode, if in PWM mode the inductor current falls below a certain threshold. The typical output current threshold depends on VIN and can be calculated according to Equation 1 for each converter.

Equation 1: Average output current threshold to enter PFM Mode

$$I_{OUT\_PFM\_enter} = \frac{VIN_{DCDC}}{32\ \Omega} \tag{1}$$

Equation 2: Average output current threshold to leave PFM Mode

$$I_{OUT\_PFM\_leave} = \frac{VIN_{DCDC}}{24\ \Omega} \tag{2}$$

In order to keep the output voltage ripple in Power Save Mode low, the output voltage is monitored with a single threshold comparator (skip comparator). As the output voltage falls below the skip comparator threshold (skip comp) of 1.01 x VOUTnominal, the corresponding converter starts switching for a minimum time period of typically 1µs and provides current to the load and the output capacitor. Therefore the output voltage increases and the device maintains switching until the output voltage trips the skip comparator threshold (skip comp) again. At this moment all switching activity is stopped and the quiescent current is reduced to minimum. The load is supplied by the output capacitor until the output voltage has dropped below the threshold again.

DETAILED DESCRIPTION (continued)

Hereupon the device starts switching again. The Power Save Mode is exited and PWM Mode entered in case the output current exceeds the current IOUT_PFM_leave, or if the output voltage falls below a second comparator threshold, called skip comparator low (Skip Comp Low) threshold. This skip comparator low threshold is set to –2% below nominal Vout, and enables a fast transition from Power Save Mode to PWM Mode during a load step. In Power Save Mode the quiescent current is reduced typically to 19µA for one converter and 32µA for both converters active. This single skip comparator threshold method in Power Save Mode results in a very low output voltage ripple. The ripple depends on the comparator delay and the size of the output capacitor. Increasing output capacitor values minimizes the output ripple. The Power Save Mode can be disabled through the MODE/DATA pin set to high. Both converters then operate in fixed PWM mode. Power Save Mode Enable/Disable applies to both converters.

Dynamic Voltage Positioning

This feature reduces the voltage under/overshoots at load steps from light to heavy load and vice versa. It is activated in Power Save Mode operation. It provides more headroom for both the voltage drop at a load step, and the voltage increase at a load throw-off. This improves load transient behavior.

At light loads, in which the converter operate in PFM Mode, the output voltage is regulated typically 1% higher than the nominal value. In case of a load transient from light load to heavy load, the output voltage drops until it reaches the skip comparator low threshold set to –2% below the nominal value and enters PWM mode. During a load throw off from heavy load to light load, the voltage overshoot is also minimized due to active regulation turning on the N-channel switch.

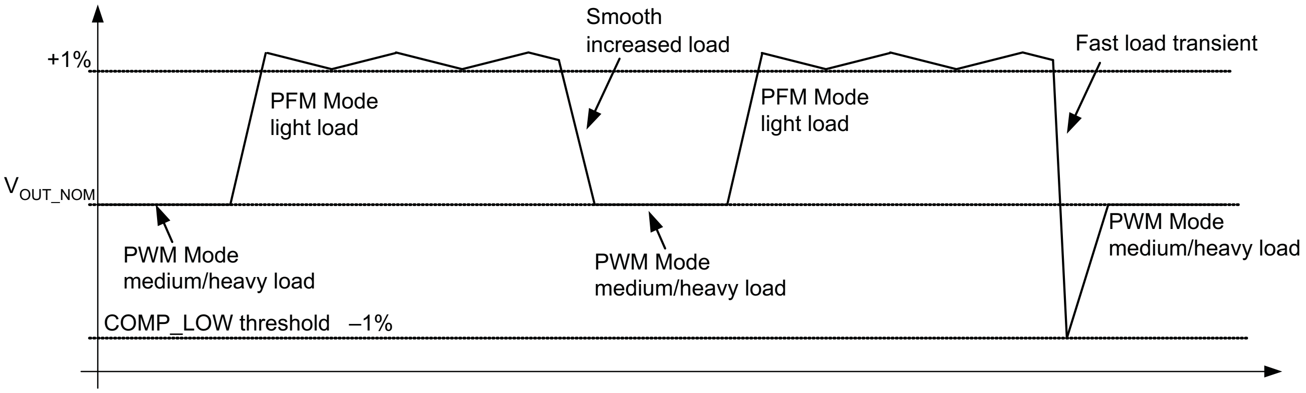


Figure 25. Dynamic Voltage Positioning

Soft Start

The two converters have an internal soft start circuit that limits the inrush current during start-up. During soft start, the output voltage ramp up is controlled as shown in Figure 26.

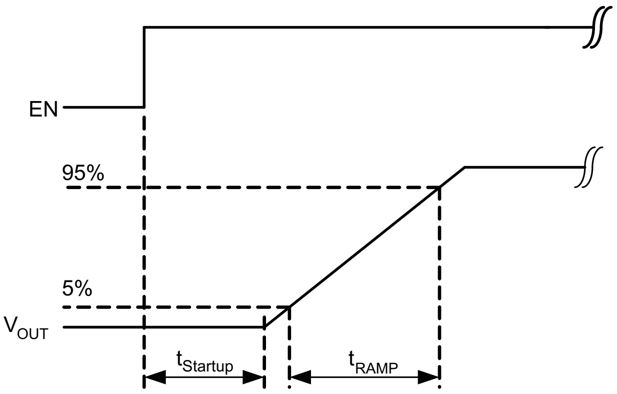


Figure 26. Soft Start

DETAILED DESCRIPTION (continued)

100% Duty Cycle Low Dropout Operation

The converters offer a low input to output voltage difference while still maintaining operation with the use of the 100% duty cycle mode. In this mode the P-channel switch is constantly turned on. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range; i.e., the minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$Vin_{min} = Vout_{max} + Iout_{max} \times \left(RDSon_{max} + R_L\right) \tag{3}$$

With:

$Iout_{max}$ = maximum output current plus inductor ripple current
$RDSon_{max}$ = maximum P-channel switch RDSon
R_L = DC resistance of the inductor
$Vout_{max}$ = nominal output voltage plus maximum output voltage tolerance

With decreasing load current, the device automatically switches into pulse skipping operation in which the power stage operates intermittently based on load demand. By running cycles periodically the switching losses are minimized and the device runs with a minimum quiescent current maintaining high efficiency.

Under-Voltage Lockout

The under voltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery and disables the converters. The under-voltage lockout threshold is typically 1.5V, max 2.35V. In case the default register values are overwritten by the Interface, the new values in the registers REG_DEF_1_Low and REG_DEF_2 remain valid as long the supply voltage does not fall under the under-voltage lockout threshold, independent of whether the converters are disabled.

MODE SELECTION

The MODE/DATA pin allows mode selection between forced PWM Mode and Power Save Mode for both converters. Furthermore, this pin is a multipurpose pin and provides (besides Mode selection) a one-pin interface to receive serial data from a host to set the output voltage. This is described in the section EasyScale Interface.

Connecting this pin to GND enables the automatic PWM and power save mode operation. The converters operate in fixed-frequency PWM mode at moderate to heavy loads and in the PFM mode during light loads, maintaining high efficiency over a wide load current range.

Pulling the MODE/DATA pin high forces both converters to operate constantly in the PWM mode even at light load currents. The advantage is the converters operate with a fixed frequency that allows simple filtering of the switching frequency for noise sensitive applications. In this mode, the efficiency is lower compared to the power save mode during light loads. For additional flexibility it is possible to switch from Power Save Mode to forced PWM mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.

In case the operation mode will be changed from forced PWM mode (MODE/DATA = high) to Power Save Mode Enable (MODE/DATA = 0) the Power Save Mode will be enabled after a delay time of typically $t_{timeout}$, which is a maximum of 520μs.

The forced PWM Mode operation is enabled immediately with Pin MODE/DATA set to 1.

ENABLE

The device has for each converter a separate EN pin to start up each converter independently. If EN1, EN2 are set to high, the corresponding converter starts up with soft start as previously described.

Pulling EN1 and EN2 pin low forces the device into shutdown, with a shutdown quiescent current of typically 1.2μA. In this mode, the P and N-Channel MOSFETs are turned-off and the entire internal control circuitry is switched-off. For proper operation the EN1 and EN2 pins must be terminated and must not be left floating.

DETAILED DESCRIPTION (continued)

DEF_1 PIN FUNCTION

The DEF_1 pin is dedicated to converter 1 and works as an analog input for adjustable output voltage setting. Connecting an external resistor network to this pin adjusts the default output voltage to any value starting from 0.6V to V_{IN}.

180° OUT OF PHASE OPERATION

In PWM Mode the converters operate with a 180° turn-on phase shift of the PMOS (high side) transistors. It prevents the high side switches of both converters to be turned on simultaneously, and therefore smooths the input current. This feature reduces the surge current drawn from the supply.

SHORT-CIRCUIT PROTECTION

Both outputs are short-circuit protected with maximum output current = I_{LIMF}(P-MOS and N-MOS). Once the PMOS switch reaches its current limit, it will be turned off and the NMOS turned on. The PMOS only turns on again, once the current in the NMOS decreases below the NMOS current limit.

THERMAL SHUTDOWN

As soon as the junction temperature, T_J, exceeds typically 150°C the device goes into thermal shutdown. In this mode, the P and N-Channel MOSFETs are turned-off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis again.

EasyScale™: One Pin Serial Interface for Dynamic Output Voltage Adjustment

General

EasyScale is a simple but very flexible one pin interface to configure the output voltage of both DC/DC converters. The interface is based on a master – slave structure, where the master is typically a µController or Application processor. Figure 27 and Table 2 give an overview of the protocol. The protocol consists of a device specific address byte and a data byte. The device specific address byte is fixed to 4E hex. The data byte consists of five bit for information, two address bits and the RFA bit. RFA bit set to high indicates the **R**equest **F**or **A**cknowledge condition. The Acknowledge condition is only applied if the protocol was received correctly.

The advantage of EasyScale compared to other one-pin interfaces is that its bit detection is, to a large extent, independent from the bit transmission rate. It can automatically detect bit rates between 1.7kBit/sec and up to 160kBit/sec. Furthermore, the interface is shared with the Mode/Data Pin and requires therefore no additional pin.

Protocol

All bits are transmitted MSB first and LSB last. Figure 28 shows the protocol without acknowledge request (bit RFA = 0), Figure 29 with acknowledge (bit RFA = 1) request.

Prior to both bytes, device address byte and data byte, a start condition needs to be applied. For this, the Mode/Data pin needs to be pulled high for at least t_{Start} before the bit transmission starts with the falling edge. In case the Mode/Data line was already at high level (forced PWM Mode selection) no start condition need be applied prior the device address byte.

The transmission of each byte needs to be closed with an End Of Stream condition for at least T_{EOS}.

Addressable Registers

In TPS62410 two registers with a data content of 5 bits can be addressed to change the output voltage of both converters. With 5 bit data content, 32 different values for each register are available. Table 1 shows the addressable registers if DEF_1 pin acts as analog input with external resistors connected.

The available output voltages for converter 1 are shown in Table 3, for converter 2 in Table 4. To generate these output voltages, a precise internal resistor divider network is used, which makes external resistors unnecessary and results therefore in an higher output voltage accuracy and less board space.

DETAILED DESCRIPTION (continued)

The Interface is activated if at least one of the converters is enabled (EN1 or EN2 is high). After the Startup-time t_{Start} (170µs) the interface is ready for data reception.

Table 1. Addressable Registers for Adjustable Output Voltage Devices

REGISTER	DESCRIPTION	A1	A0	D4	D3	D2	D1	D0
REG_DEF_1_High	Not available in TPS62410 adjustable version	0	1					
REG_DEF_1_Low	Converter 1 output voltage setting	0	0	TPS62410 see Table 3				
REG_DEF_2	Converter 2 output voltage	1	0	TPS62410 see Table 4, connect ADJ2 pin directly to $VOUT_2$				
	Don’t use	1	1					

Bit Decoding

The bit detection is based on a PWM scheme, where the criterion is the relation between t_{LOW} and t_{HIGH}. It can be simplified to:

High Bit: $t_{High} > t_{Low}$, but with t_{High} at least 2x t_{Low}, see Figure 30
Low Bit: tLow> tHigh, but with tLow at least 2x tHigh, see Figure 30

The bit detection starts with a falling edge on the MODED/DATA pin and ends with the next falling edge. Depending on the relation between t_{Low} and t_{High} a 0 or 1 is detected.

Acknowledge

The Acknowledge condition is only applied if:

- Acknowledge is requested by a set RFA bit
- The transmitted device address matches with the device address of the device
- 16 bits were received correctly

In this case, the device turns on the internal ACKN-MOSFET and pulls the MODE/DATA pin low for the time tACKN, which is max. 520µs. The Acknowledge condition is valid after an internal delay time t_{valACK}. This means the internal ACKN-MOSFET is turned on after t_{valACK}, when the last falling edge of the protocol was detected. The master controller keeps the line low during this time.

The master device can detect the acknowledge condition with it’s input by releasing the MODE/DATA pin after tvalACK and read back a 0.

In case of an invalid device address or not correctly received protocol, no acknowledge condition will be applied, thus the internal MOSFET will not be turned on and the external pullup resistor pulls MODE/DATA pin high after t_{valACK}. The MODE/DATA pin can be used again after the acknowledge condition ends.

NOTE:

The acknowledge condition may only be requested in case the master device has an open drain output.

In case of a push pull output stage it is recommended to use a series resistor in the MODE/DATA line to limit the current to 500µA in case of an accidentally requested acknowledge to protect the internal ACKN-MOSFET.

MODE Selection

Because of the MODE/DATA pin is used for two functions, interface and a MODE selection, the device needs to determine when it has to decode the bit stream or to change the operation mode.

The device enters forced PWM mode operation immediately whenever the MODE/DATA pin turns to high level. The device stays also in forced PWM mode during the whole time of a protocol reception.

With a falling edge on the MODE/DATA pin the device starts bit decoding. If the MODE/DATA pin stays low for at least $t_{timeout}$, the device get’s an internal timeout and Power Save Mode operation is enabled.

A protocol which is sent within this time will be ignored, because the falling edge for the Mode change will be first interpreted as start of the first bit. In this case it is recommended to send first the protocol and change at the end of the protocol to Power Save Mode.

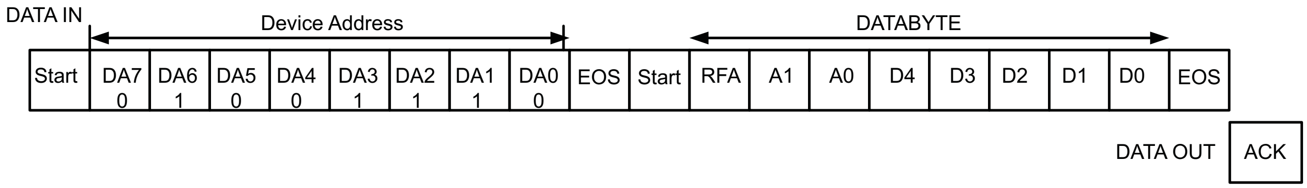


Figure 27. Easy Scale Protocol Overview

Table 2. Easy Scale Bit Description

BYTE	BIT NUMBER	NAME	TRANSMISSION DIRECTION	DESCRIPTION
Device Address Byte 4Ehex	7	DA7	IN	0 MSB device address
	6	DA6	IN	1
	5	DA5	IN	0
	4	DA4	IN	0
	3	DA3	IN	1
	2	DA2	IN	1
	1	DA1	IN	1
	0	DA0	IN	0 LSB device address
Databyte	7(MSB)	RFA	IN	Request For Acknowledge, if high, Acknowledge condition will applied by the device
	6	A1		Address Bit 1
	5	A0		Address Bit 0
	4	D4		Data Bit 4
	3	D3		Data Bit 3
	2	D2		Data Bit 2
	1	D1		Data Bit 1
	0(LSB)	D0		Data Bit 0
		ACK	OUT	Acknowledge condition active 0, this condition will only be applied in case RFA bit is set. Open drain output, Line needs to be pulled high by the host with a pullup resistor. This feature can only be used if the master has an open drain output stage. In case of a push pull output stage Acknowledge condition may not be requested!

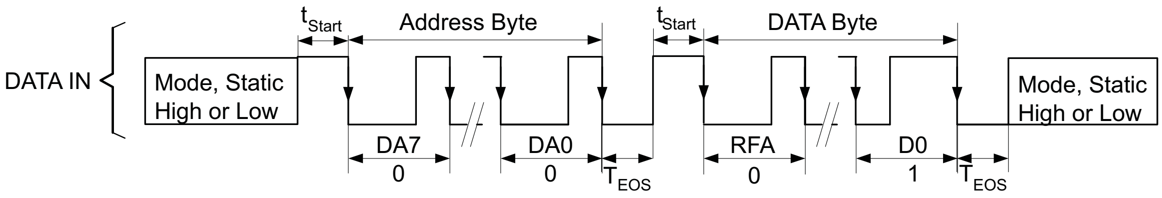


Figure 28. Easy Scale Protocol Without Acknowledge

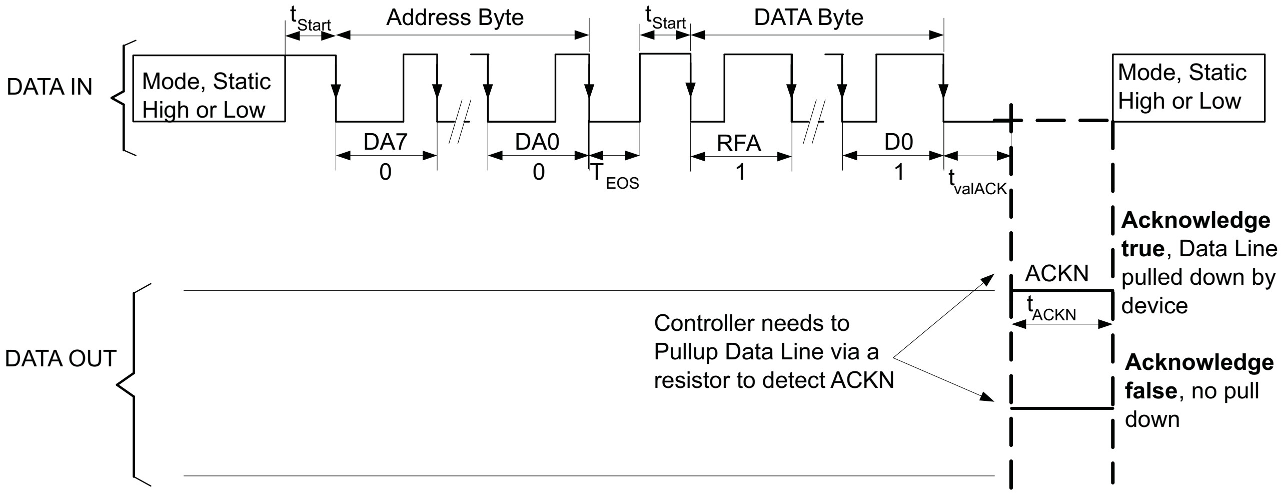


Figure 29. Easy Scale Protocol Including Acknowledge

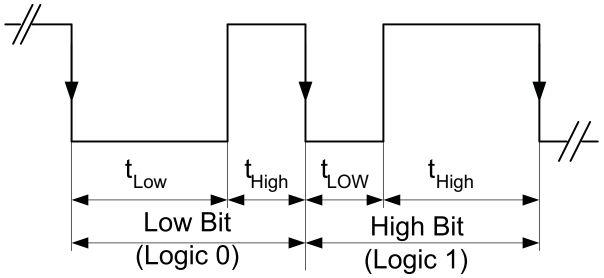


Figure 30. EasyScale – Bit Coding

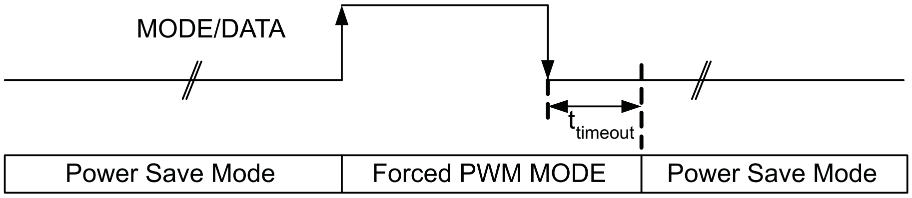


Figure 31. MODE/DATA PIN: Mode Selection

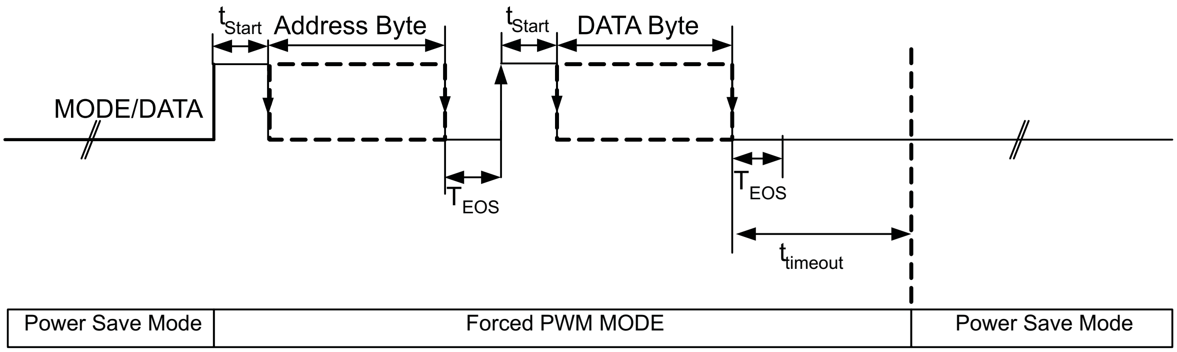


Figure 32. MODE/DATA Pin: Power Save Mode/Interface Communication

Table 3. Selectable Output Voltages for Converter 1, With DEF1 Pin as Analog Input (TPS62410)

	TPS62410 OUTPUT VOLTAGE [V] REGISTER REG_DEF_1_LOW	D4	D3	D2	D1	D0
0	**V_{OUT1} Adjustable Output With Resistor Network on DEF_1 Pin**	**0**	**0**	**0**	**0**	**0**
	0.6V with DEF_1 Pin connected to V_{OUT1}					
1	0.825	0	0	0	0	1
2	0.85	0	0	0	1	0
3	0.875	0	0	0	1	1
4	0.9	0	0	1	0	0
5	0.925	0	0	1	0	1
6	0.95	0	0	1	1	0
7	0.975	0	0	1	1	1
8	1.0	0	1	0	0	0
9	1.025	0	1	0	0	1
10	1.050	0	1	0	1	0
11	1.075	0	1	0	1	1
12	1.1	0	1	1	0	0
13	1.125	0	1	1	0	1
14	1.150	0	1	1	1	0
15	1.175	0	1	1	1	1
16	1.2	1	0	0	0	0
17	1.225	1	0	0	0	1
18	1.25	1	0	0	1	0
19	1.275	1	0	0	1	1
20	1.3	1	0	1	0	0
21	1.325	1	0	1	0	1
22	1.350	1	0	1	1	0
23	1.375	1	0	1	1	1
24	1.4	1	1	0	0	0
25	1.425	1	1	0	0	1
26	1.450	1	1	0	1	0
27	1.475	1	1	0	1	1
28	1.5	1	1	1	0	0
29	1.525	1	1	1	0	1
30	1.55	1	1	1	1	0
31	1.575	1	1	1	1	1

Table 4. Selectable Output Voltages for Converter 2, (ADJ2 Connected to V_{OUT})

	OUTPUT VOLTAGE [V] FOR REGISTER REG_DEF_2	**D4**	**D3**	**D2**	**D1**	**D0**
0	**V_{OUT2} Adjustable Output With Resistor Network on ADJ2**	**0**	**0**	**0**	**0**	**0**
	0.6V with ADJ2 Pin connected to V_{OUT2}					
1	0.85	0	0	0	0	1
2	0.9	0	0	0	1	0
3	0.95	0	0	0	1	1
4	1.0	0	0	1	0	0
5	1.05	0	0	1	0	1
6	1.1	0	0	1	1	0
7	1.15	0	0	1	1	1
8	1.2	0	1	0	0	0
9	1.25	0	1	0	0	1
10	1.3	0	1	0	1	0
11	1.35	0	1	0	1	1
12	1.4	0	1	1	0	0
13	1.45	0	1	1	0	1
14	1.5	0	1	1	1	0
15	1.55	0	1	1	1	1
16	1.6	1	0	0	0	0
17	1.7	1	0	0	0	1
18	1.8	1	0	0	1	0
19	1.85	1	0	0	1	1
20	2.0	1	0	1	0	0
21	2.1	1	0	1	0	1
22	2.2	1	0	1	1	0
23	2.3	1	0	1	1	1
24	2.4	1	1	0	0	0
25	2.5	1	1	0	0	1
26	2.6	1	1	0	1	0
27	2.7	1	1	0	1	1
28	2.8	1	1	1	0	0
29	2.85	1	1	1	0	1
30	3.0	1	1	1	1	0
31	3.3	1	1	1	1	1

APPLICATION INFORMATION

OUTPUT VOLTAGE SETTING

Converter1 Adjustable Default Output Voltage Setting

The output voltage can be calculated to:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{11}}{R_{12}}\right) \text{ with an internal reference voltage } V_{REF} \text{ typical 0.6V} \quad (4)$$

To keep the operating current to a minimum, it is recommended to select R_{12} within a range of 180kΩ to 360kΩ. The sum of R_{12} and R_{11} should not exceed ~1MΩ. For higher output voltages than 3.3V, it is recommended to choose lower values than 180kΩ for R12. Route the DEF_1 line away from noise sources, such as the inductor or the SW1 line. The FB1 line needs to be directly connected to the output capacitor. An internal feed forward capacitor is connected to this pin, therefore there is no need for an external feed forward capacitor for converter 1.

Converter 2

The default output voltage of converter 2 can be set by an external resistor network. For converter 2 the same recommendations apply as for converter 1. In addition to that, a 33pF external feed forward capacitor C_{ff2} for good load transient response must be used.

The output voltage can be calculated to:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{21}}{R_{22}}\right) \text{ with an internal reference voltage } V_{REF} \text{ typical 0.6V} \quad (5)$$

Route the ADJ2 line away from noise sources, such as the inductor or the SW2 line. In case the interface is used for converter 2, connect ADJ2 pin directly to V_{OUT2}

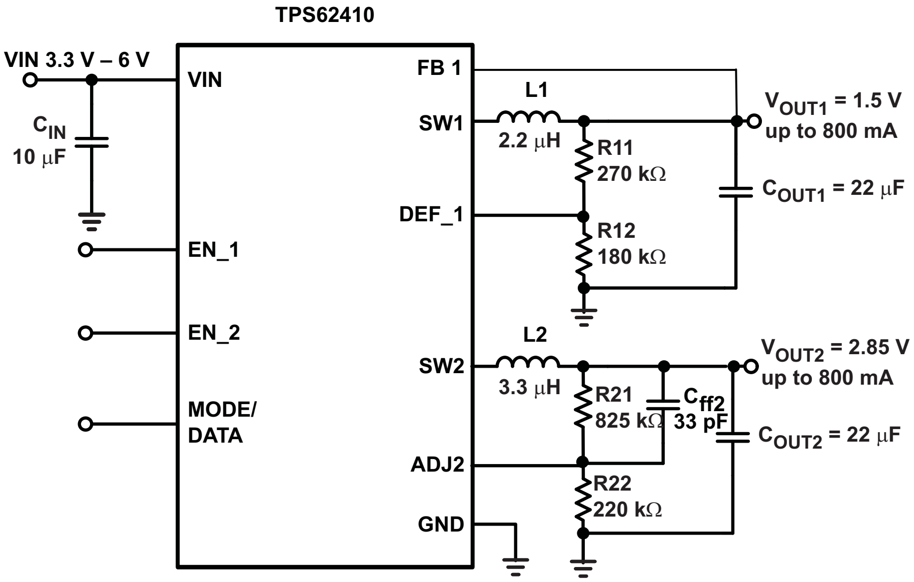


Figure 33. Typical Application Circuit 1.5V/2.85V Adjustable Outputs, low PFM Voltage ripple Optimized

APPLICATION INFORMATION (continued)

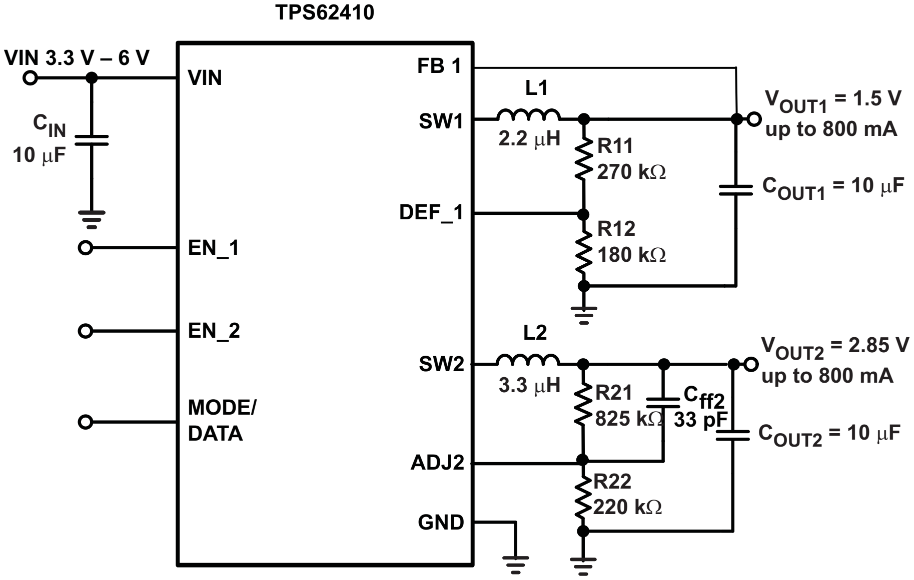


Figure 34. Typical Application Circuit 1.5V/2.85V Adjustable Outputs

OUTPUT FILTER DESIGN (INDUCTOR AND OUTPUT CAPACITOR)

The device is optimized to operate with inductors of 2.2µH to 4.7µH and output capacitors of 10µF to 22µF.

For operation with a 2.2µH inductor, a 22µF capacitor is suggested.

Inductor Selection

The selected inductor has to be rated for its DC resistance and saturation current. The DC resistance of the inductance will influence directly the efficiency of the converter. Therefore an inductor with lowest DC resistance should be selected for highest efficiency.

Equation 6 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 7. This is recommended because during heavy load transient the inductor current will rise above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \tag{6}$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \tag{7}$$

With:

f = Switching Frequency (2.25MHz typical)

L = Inductor Value

ΔI_L= Peak to Peak inductor ripple current

I_{Lmax} = Maximum Inductor current

The highest inductor current will occur at maximum Vin.

Open core inductors have a soft saturation characteristic and they can usually handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. It must be considered, that the core material from inductor to inductor differs and will have an impact on the efficiency especially at high switching frequencies.

APPLICATION INFORMATION (continued)

Refer to Table 5 and the typical applications for possible inductors.

Table 5. List of Inductors

DIMENSIONS [mm^3]	INDUCTOR TYPE	SUPPLIER
2.8x2.6×1.4	VLF3014	TDK
3×3×1.4	LPS3015	Coilcraft
3.9×3.9×1.7	LPS4018	Coilcraft

Output Capacitor Selection

The advanced fast response voltage mode control scheme of the two converters allows the use of small ceramic capacitors with a typical value of 10µF, without having large output voltage under and overshoots during heavy load transients. Ceramic X7R/X5R capacitors having low ESR values result in lowest output voltage ripple and are therefore recommended.

If ceramic output capacitors are used, the capacitor RMS ripple current rating will always meet the application requirements. The RMS ripple current is calculated as:

$$I_{RMSCout} = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \tag{8}$$

At nominal load current the inductive converters operate in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta Vout = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \left(\frac{1}{8 \times Cout \times f} + ESR\right) \tag{9}$$

Where the highest output voltage ripple occurs at the highest input voltage Vin.

At light load currents the converters operate in Power Save Mode and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. Higher output capacitors like 22µF values minimize the voltage ripple in PFM Mode and tighten DC output accuracy in PFM Mode.

Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. The converters need a ceramic input capacitor of 10µF. The input capacitor can be increased without any limit for better input voltage filtering.

LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues as well as EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths as indicated in bold in Figure 35.

The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor.

Connect the GND Pin of the device to the PowerPAD of the PCB and use this Pad as a star point. For each converter use a common Power GND node and a different node for the Signal GND to minimize the effects of ground noise. Connect these ground nodes together to the PowerPAD (star point) underneath the IC. Keep the common path to the GND PIN, which returns the small signal components and the high current of the output capacitors as short as possible to avoid ground noise. The output voltage sense lines (FB 1, ADJ2, DEF_1) should be connected right to the output capacitor and routed away from noisy components and traces (e.g., SW line). If the EasyScale interface is operated with high transmission rates, the MODE/DATA trace must be routed away from the ADJ2 line to avoid capacitive coupling into the ADJ2 pin. A GND guard ring between the MODE/DATA pin and ADJ2 pin avoids potential noise coupling.

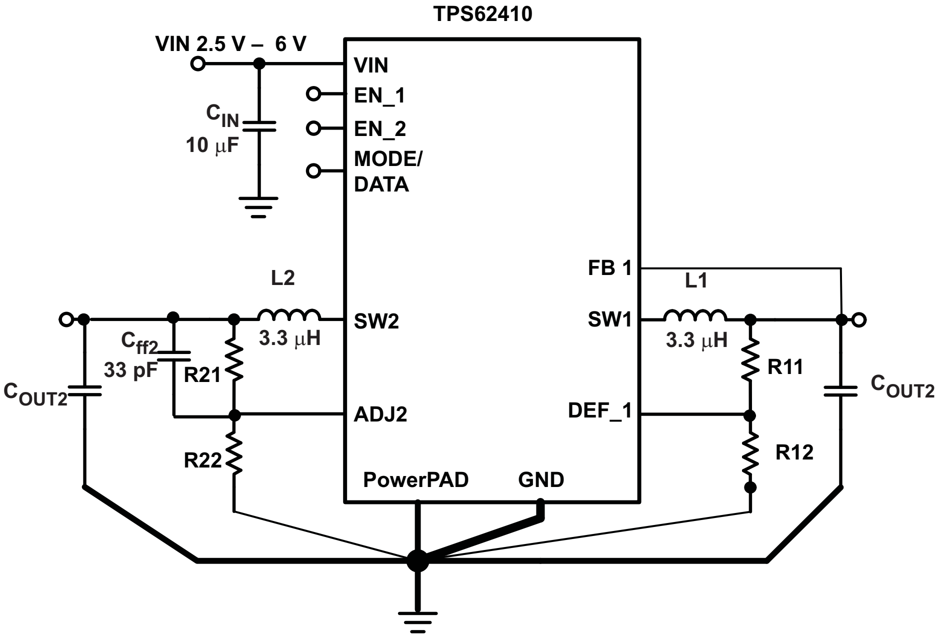


Figure 35. Layout Diagram

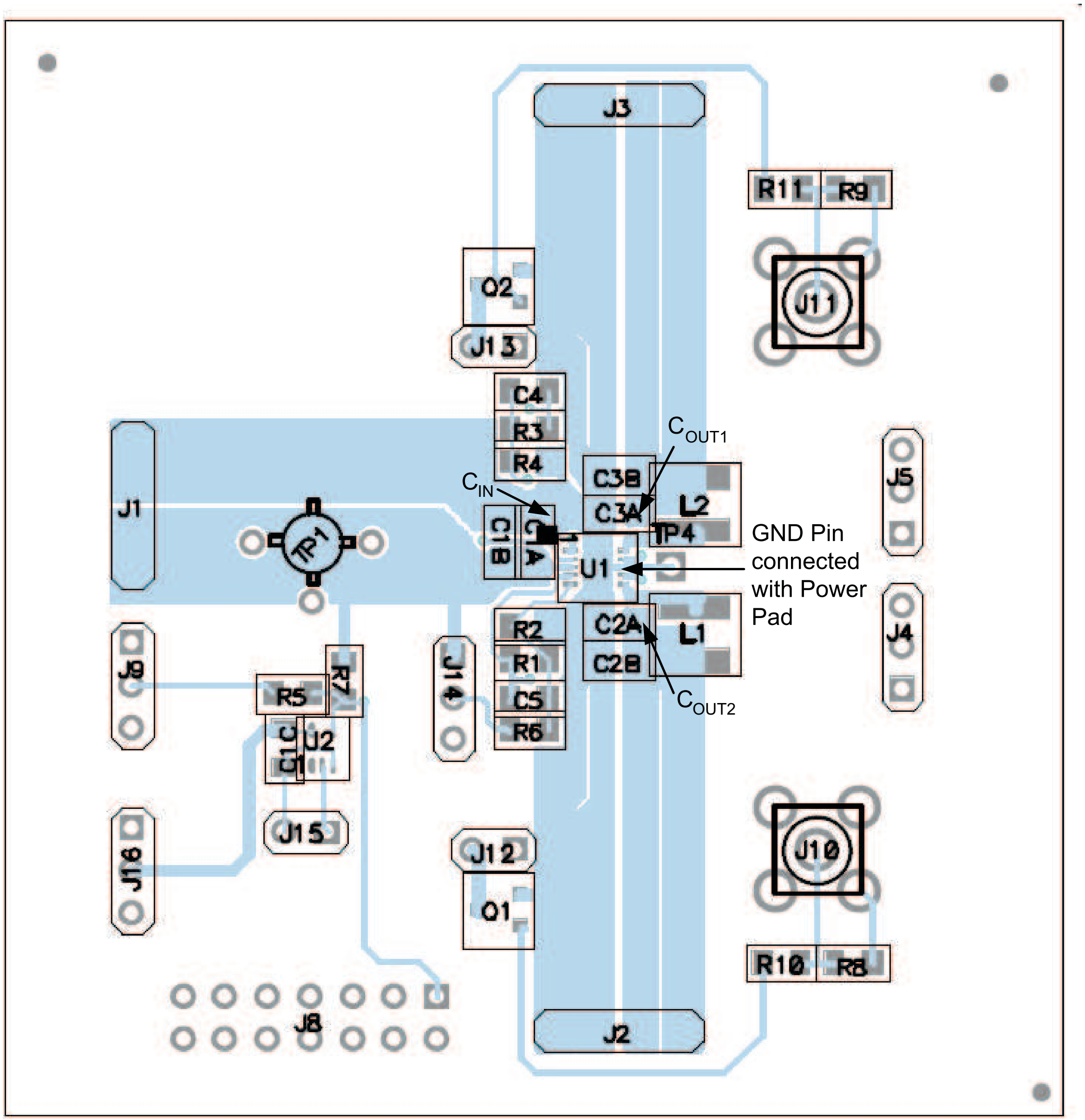
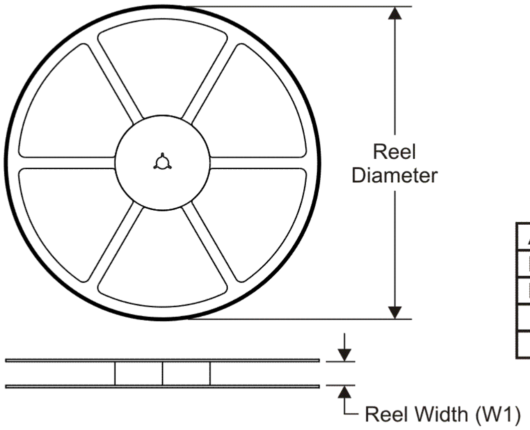


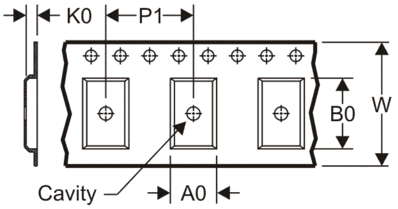
Figure 36. PCB Layout

TAPE AND REEL INFORMATION

REEL DIMENSIONS

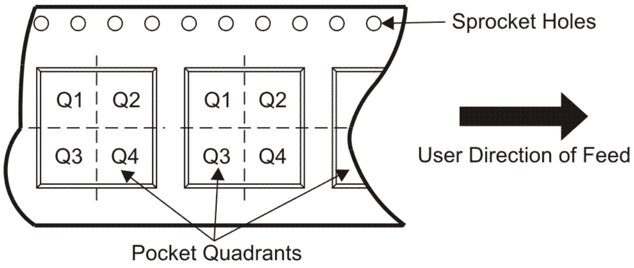


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

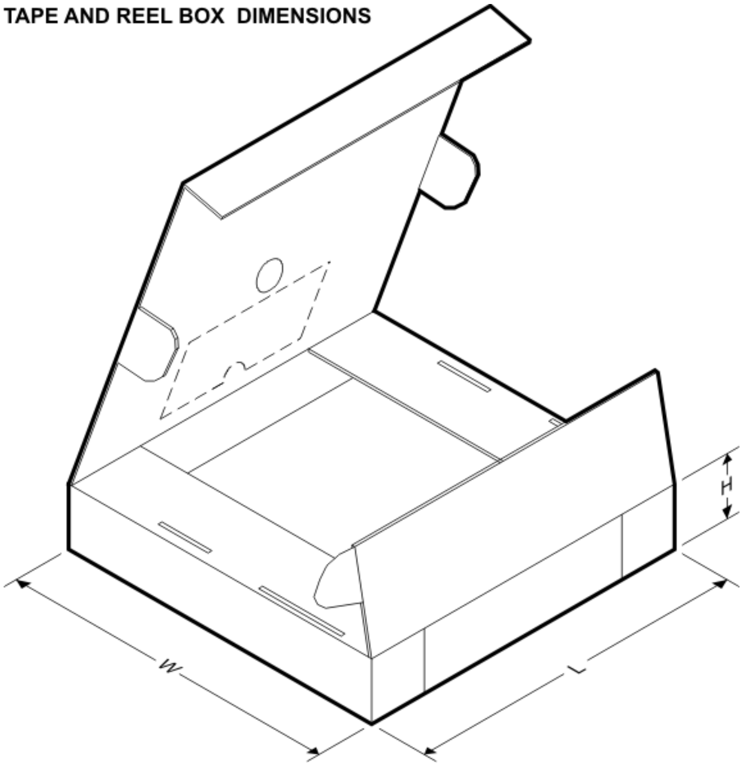
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62410DRCR	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62410DRCT	SON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

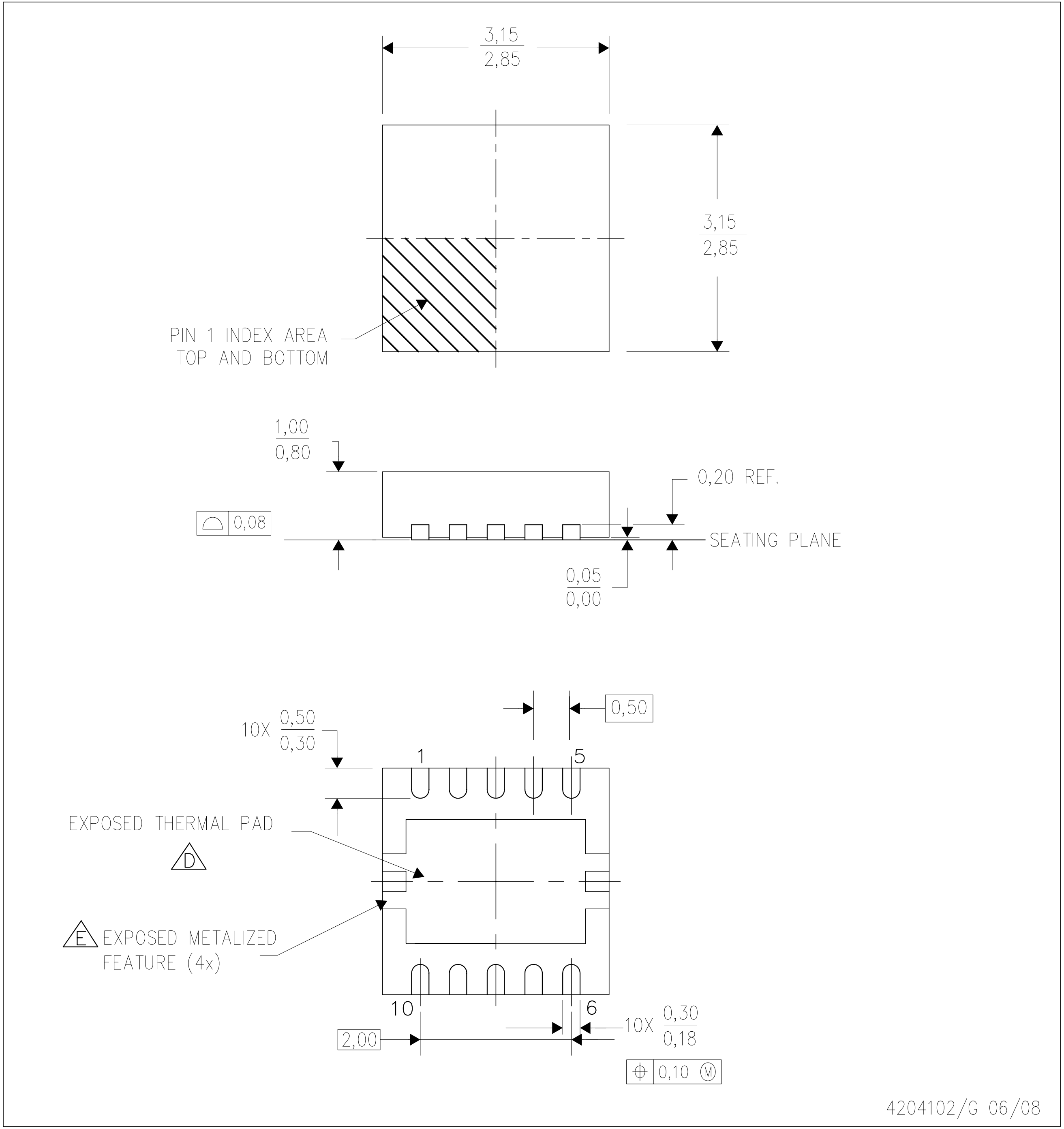
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62410DRCR	SON	DRC	10	3000	346.0	346.0	29.0
TPS62410DRCT	SON	DRC	10	250	190.5	212.7	31.8

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



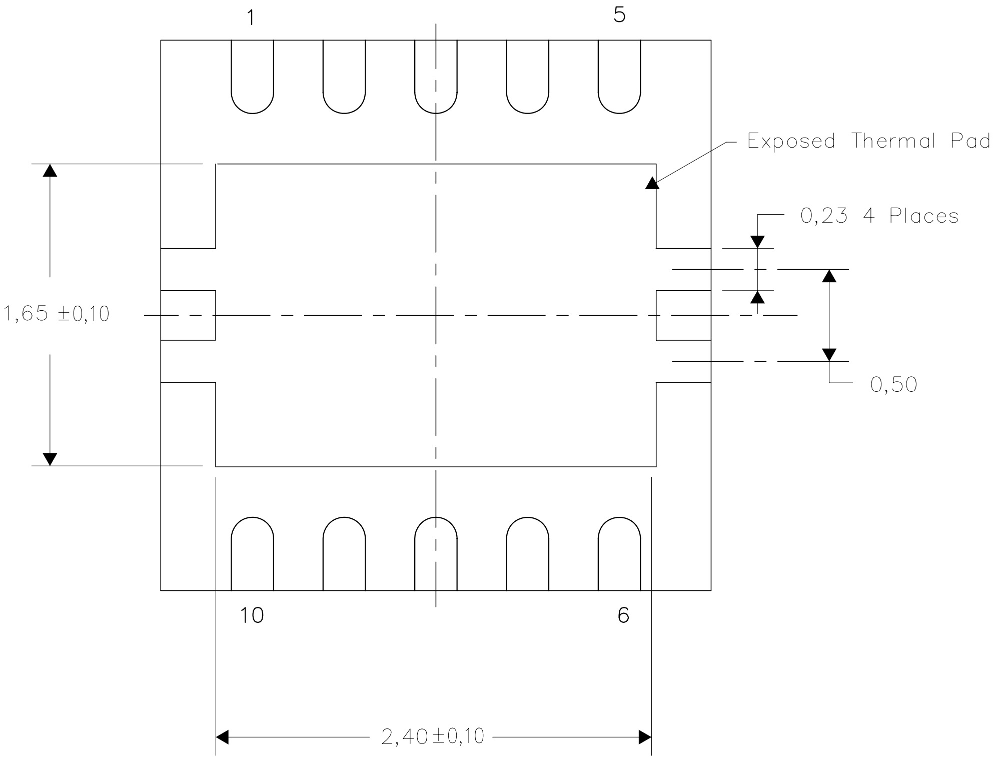
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No–Lead (SON) package configuration.
- D The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. Metalized features are supplier options and may not be on the package.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

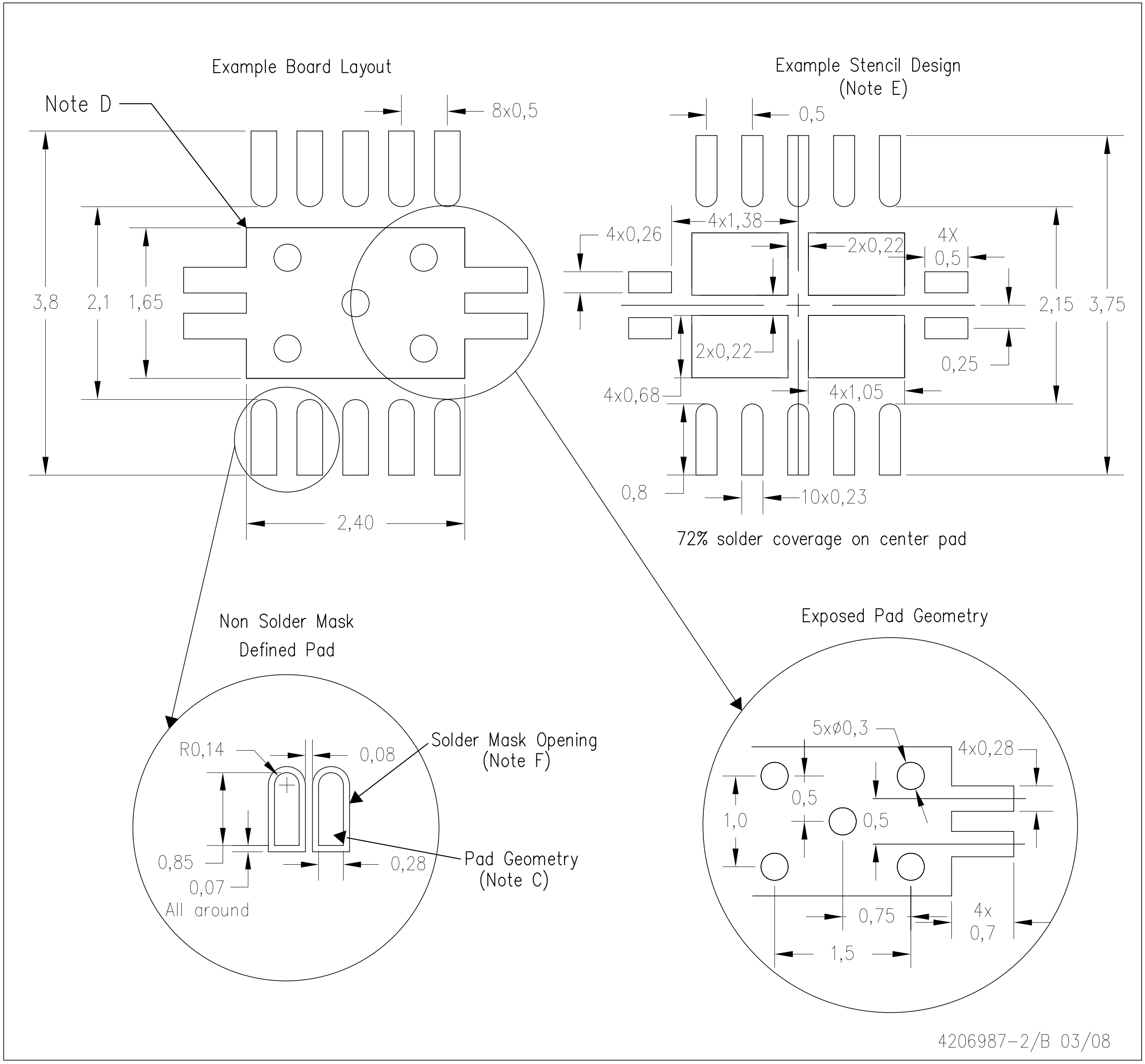


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRC (S–PVSON–N10)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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